REMARKS

I. Introduction

In response to the Office Action dated December 10, 2007, Applicants have amended claims 1, 5, and 6. Claim 3 has been canceled. Care has been taken to avoid the introduction of new matter. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Objections

Applicants have amended the typographical error in claim 5 as suggested by the Examiner. Accordingly, withdrawal of the claim objection is requested.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 2 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Tojima (U.S. 2002/0026543) in view of Shitara (U.S. 5,430,844). Claims 3 – 6 stand rejected under § 103(a) as allegedly being unpatentable over Tojima in view of Shitara and Coke. Applicants traverse these rejections for at least the following reasons.

Claim 1 recites, among other things, a DMA controller capable of generating ring buffer addresses which comprises a third register, and which in said first mode of operation, contains the difference between the end address and the start address of the ring buffer, wherein, in a second mode of operation the third register sets the address increment of a non-contiguous area in the DMA transfer of a rectangular area. Thus, the structure recited in claim 1 provides two modes of operation, enabling a DMA controller to transfer data in non-contiguous areas (such as a rectangular block transfer) and ring buffer transfer, without adding circuits dedicated to the ring buffer, such as start address and end address registers and a comparator (see, Specification, pp. 6-7). At least these features are not disclosed by any of the cited references, alone or in combination with each other.

The Examiner acknowledges that Tojima does not disclose having a third register which stores the difference between the end address and the start address of the ring buffer, and relies on Shitara to overcome this deficiency. The Examiner asserts that Shitara discloses that it is well known in the art that DMA transfers require the size of the total DMA transfer. The Examiner further cites col. 1, lines 58 – 62 of Shitara for the disclosure that DMA transfer generally requires two registers, one for address and another for size. The Examiner concludes that because Shitara discloses storing the start address and the size of the transfer, there is no need for the end address as this would be a matter of design choice. Applicants submit, however, that claim 1 includes a first register which stores the start address and a second register which stores the number of transfers from start to end, in addition to the third register which stores the difference between the start and end address registers in the first mode of operation.

Moreover, claim 1 also recites that the third register sets the address increment of a non-contiguous area in the DMA transfer of a rectangular area. In reference to now canceled claim 3, the Examiner acknowledges that Tojima and Shitara fail to disclose the address increment of a non-contiguous area and asserts that Coke overcomes this deficiency. Thus, while the Examiner argues that a third register for storing the difference between the end address and the start address is not needed (see p. 3 of the Office Action), the Examiner also asserts that Coke teaches a third register used as a register for setting the address increment of a non-contiguous area in the DMA transfer of a rectangular area. However, neither Shitara nor Coke provide a suggestion for including a third register in Tojima as described above. Coke appears to disclose a DMA circuit wherein data stored at non-sequential addresses in memory can be transferred. Coke does not disclose a first mode of operation and a second mode of operation. As such, Coke cannot disclose or suggest a register that stores the difference between the end address and the start

address of the ring buffer in first mode and sets the address increments of a non-contiguous area to the third register in a second mode.

Regarding claim 5, the Examiner acknowledges that Tojima and Shitara fail to disclose means for setting the address increment of a non-contiguous area to a third register. The Examiner relies on Coke as allegedly teaching setting the address increment of a non-contiguous area to the third register, asserting that it would have been obvious to one of ordinary skill in the art to combine the size/length information of Shitara and the increment information of Coke with the DMA controller of Tojima in order to reduce the processor load on the system.

Claim 5 is directed to a computer readable medium encoded with a computer program which causes a computer to operate in two modes, a ring buffer transfer mode and a rectangle block transfer mode, using the same three registers. In a ring buffer transfer mode, the second register is used to set the number of DMA transfers from the start address to the end address of the ring buffer and the third register is used to store the difference between the end address and the start address of the ring buffer. In the rectangle block transfer mode, the second register is used to set the number of DMA transfers in a contiguous area including rectangular areas and the third register is used to set the address increment of a non-contiguous area to the third register.

As set forth in response to previous rejections, none of the cited references, alone or in combination with each other, disclose or suggest a third register that stores the difference between the end address and the start address of the ring buffer in a ring buffer transfer mode and sets the address increments of a non-contiguous area to the third register in a rectangle transfer mode. As described above with reference to claim 1, the Examiner appears to be arguing that a third register for storing the difference between the end address and the start address is not needed (see p. 3 of the Office Action), while also asserting that Coke teaches a third register used

as a register for setting the address increment of a non-contiguous area in the DMA transfer of a rectangular area. However, Shitara nor Coke provide a suggestion for including a third register in Tojima as described above. Coke appears to disclose a DMA circuit wherein data stored at non-sequential addresses in memory can be transferred. Coke does not disclose ring buffer transfer operations nor rectangle block transfer operations. Furthermore, Coke does not disclose or suggest a register that stores the difference between the end address and the start address of the ring buffer in a ring buffer transfer mode and sets the address increments of a non-contiguous area to the third register in a rectangular transfer mode.

Applicants would like to point out that the Examiner has once again failed to address Applicants arguments that Coke does not disclose or suggest a register that stores the difference between the end address and the start address of the ring buffer in a ring buffer transfer mode and sets the address increments of a non-contiguous area to the third register in a rectangular transfer mode. Despite the Examiner's acknowledgment in the Interview Summary dated October 1, 2007 that the rejection "did not fully explain the obviousness of using the same third register for different values for the different modes of operation," the Examiner has once again failed to make such a case for obviousness. While Applicants strongly assert that these features are not disclosed or suggested by any of the cited references, alone or in combination with each other based on the remarks provided above, if the Examiner wishes to maintain this rejection, Applicants respectfully request that all arguments be considered and addressed by the Examiner in a non-final office action.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a prima facie case of obviousness (MPEP § 2143.03), and the cited references, taken alone or in combination with each other, fail to disclose or suggest at least

the features recited above, it is respectfully submitted that independent claims 1 and 5 are patentable over the cited references.

Claims 2, 4, and 6 depend from claim 1. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Harness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for at least the reasons set forth above, it is respectfully submitted that all dependent claims are also in condition for allowance. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MWE
Facsimile: 202.756.8087
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